

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Krishna K. Nair et al;
Serial No.: not yet assigned
Filed: concurrently herewith
For: METHODS OF FORMING ELECTRONIC STRUCTURES INCLUDING
CONDUCTIVE SHUNT LAYERS AND RALATED STRUCTURES

Date: June 23, 2003

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

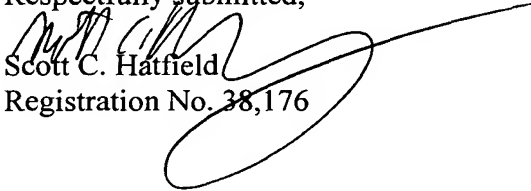
INFORMATION DISCLOSURE STATEMENT

Sir:

Attached is a list of documents on form PTO-1449 together with a copy of each identified document. It is requested that these documents be considered by the Examiner and officially made of record in accordance with the provisions of 37 C.F.R. § 1.97 and Section 609 of the MPEP.

No fee is believed due. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to our Deposit Account No. 50-0220.

Respectfully submitted,


Scott C. Hatfield

Registration No. 38,176



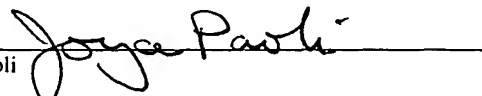
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PATENT TRADEMARK OFFICE

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Date of Deposit: June 23, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Mail Stop Patent Application, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Joyce Paoli
200733

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)				Attorney Docket Number 9180-29		Serial No. To Be Assigned	
				Applicants: Krishna K. Nair et al;			
				Filing Date: Concurrently Herewith		Group	
U. S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation Yes No
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	1.	W.J. Choi et al; <i>Electromigration of Flip Chip Solder Bump on Cu/Ni(V) Al Thin Film Under Bump Metallization</i> ; 2002 Electronic Components and Technology Conference; pp 1201-1205.					
	2.	K. Zeng et al; <i>Six cases of reliability study of Pb-free solder joints in electronic packaging technology</i> , Reports: A Review Journal; Materials Science and Engineering R 38 (2002) pp 55-105.					

 EXAMINER
 *EXAMINER

DATE CONSIDERED

Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.